ABSTRACT

The invention relates to a circuit which is integrated in a receiver system for digital television networks and which processes and routes data from one or more Motion Picture Expert Group (MPEG) data streams between two or more interfaces or peripherals, using an embedded processor (PROC) and an internal shared bus (BUS). The inventive integrated circuit comprises at the least the following integrated peripherals: two input MPEG stream interfaces (ITSINA and ITSINB); two output MPEG stream interfaces (ITSOUTA and ITSOUTB); a hard disk interface (IHD); a local network interface (ILAN); two smart card interfaces (ISMCA and ISMCB); a generic master interface to external slave peripherals and external memory (IMB); and a generic slave interface from another external master device (ISB).